In re Application of: Vaglica, John Serial No.: 10/646,081 Filed: September 19, 2001 For: CPU POWERDOWN METHOD AND APPARATUS THEREFOR	November 1, 2007 Examiner: Eric Chang Docket No.: SC11372TH

Ms. Johnson,

Thank you for pointing out the typographical errors in the appeal brief and reply brief in which 102 was mistakenly used instead of 103. In this regard, please substitute the attached pages 5 and 3 for pages 5 and 3 of the appeal brief and reply brief, respectively.

Respectfully submitted,

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Claim 21 further recites that the power control means, which is supported by power control 12 of FIG. 1, is coupled to the logic unit and receives the low power mode signal, disables the clock generator, maintains power to the logic unit while removing power from the execution unit. Receiving the low power mode signal is described at page 6, lines 9-12. Disabling the clock generator is described at page 6, lines 17-19. Maintaining and removing power is described at page 6, lines 9-12 as VD1 becoming floating and VD2 becoming reduced to a lower voltage. Since VD1 becomes floating, power is removed from the execution unit because the execution unit is powered by VD1. Since VD2 is still powered, albeit at a somewhat reduced level, power is maintained at exception logic 14 (supports claimed logic unit).

GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

Are claims 1-3, 5-21 obvious under 35 U.S.C. 103 by US Patents 5,167,024 (Smith); 6,546,472 (Atkinson); and 5,689,714 (Moyer)?

ARGUMENT

Arguments for Ground 1

Independent Claim 1

Independent claims 1, 12, and 21 stand rejected under 35 U.S.C. 103 as being obvious in view of US Patents 5,167,024 (Smith); 6,546,472 (Atkinson); and 5,689,714 (Moyer).

Smith and Atkinson both are describing a computer system that has a central processing unit (CPU). In Smith the CPU is CPU 12. In Atkinson the CPU is CPU 130. Smith even states that the CPU is preferably a "68000 based (part numbers 68000, 68020, and 68030) processor ..." Moyer is directed to a data processor (microcontroller) that has a CPU 12. The data processor of Moyer further includes a register that provides low power mode information to peripherals outside data processor 10. Applicant's independent claims 1 and 12 are directed to a data processing system and a method, respectively, having a low power mode in which, among other things, power is removed from a portion of the CPU but continued to be applied to another portion of the CPU. In particular in the low power mode, power is removed from the execution unit but

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